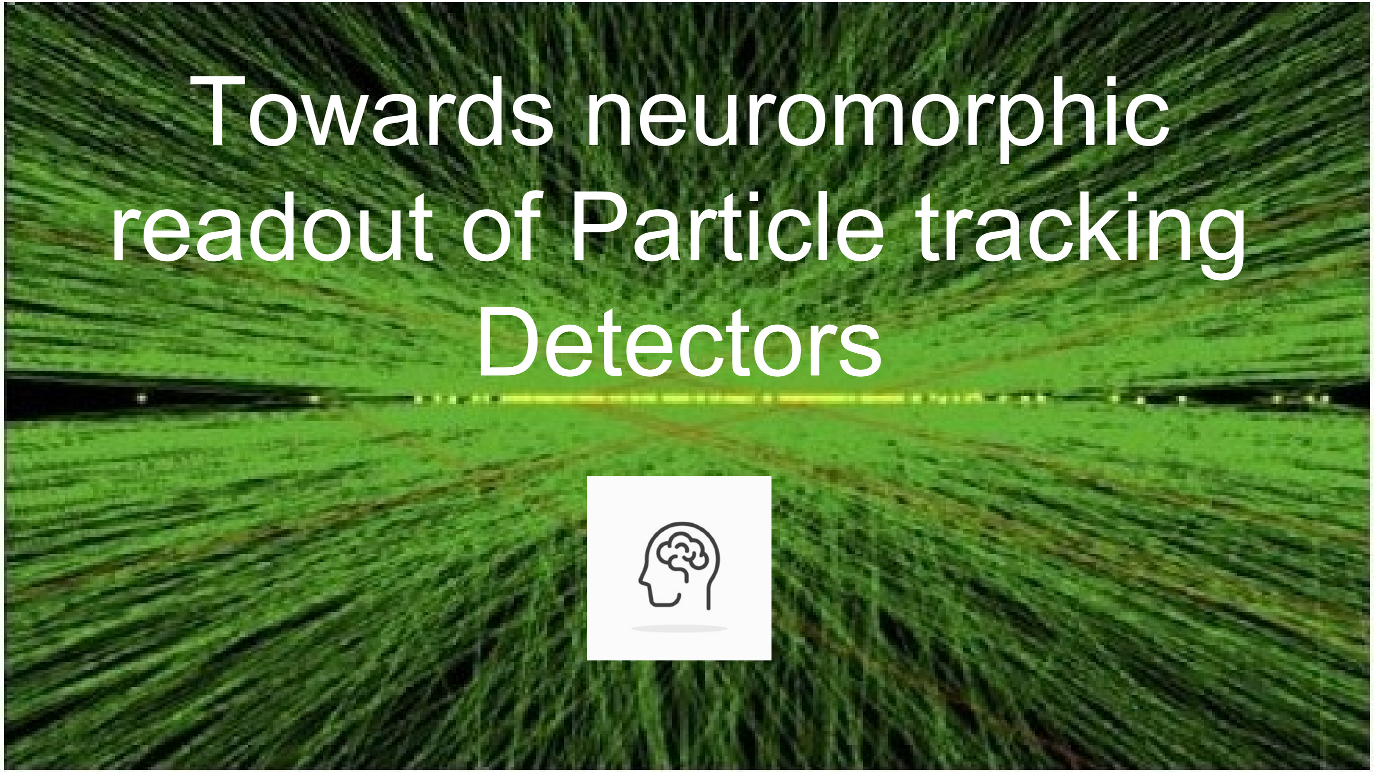
Towards neuromorphic readout of Particle tracking Detectors



Courtesy Lindsey Gray, FNAL

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January 25, 2024

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This is work in progress! I'm learning about all of this stuff. People who are helping:

Mathieu Benoit, Shruti Kulkarni, Aaron Young, Prasanna Date, Narasinga Miniskar, Jeff Vetter – ABISKO Project
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John Hopkins University

Catherine Schuman
University of Tennessee, Knoxville

Derek Grove – University of Kansas,
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References

Shruti R. Kulkarni et al., “On-sensor Data Filtering using Neuromorphic Computing for High Energy Physics Experiments”, ICONS 23 Proceedings, arXiv:2307.11242

Jieun Yoo et al., “Smart pixel sensors: towards on-sensor filtering of pixel clusters with deep learning,” arXiv: 2310.02474v (3 Oct 2023)

Manfred Krammer, Frank Hartmann, “Silicon Detectors”, https://indico.cern.ch/event/124392/contributions/1339904/attachments/74582/106976/IntroSilicon.pdf

G. Giacomini, W. Chen, G. D’Amen, and A. Tricoli, *Fabrication and performance of ACcoupled LGADs*, Journal of Instrumentation 14 no. 09, P09004–P09004 (2019).

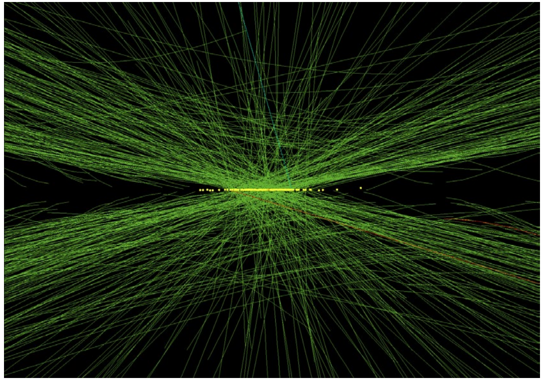
CMS Collaboration, A MIP Timing Detector for the CMS Phase-2 Upgrade, Tech. Rep. CERN-LHCC-2019-003. CMS-TDR-020, CERN, Geneva, Mar, 2019.

OUTLINE

- CMS tracking detectors
- Smart Pixel Project with Neuromorphic algorithm
- Timing detectors
- Neutron detection application

CMS Experiment at CERN

- Physics Goals are many including studying the Higgs and searching for new physics beyond the Standard Model
- Plans are to continue to ramp up luminosity and take data until 2040
- High Luminosity- LHC (HL-LHC) detector being built to start taking data in 2029
- Presently # events/25ns ~50 HL-LHC up to 200!



CMS 200PU HL-LHC Event:

Courtesy Lindsey Gray, FNAL

Need to have:

precision tracking –

measuring positions near collision

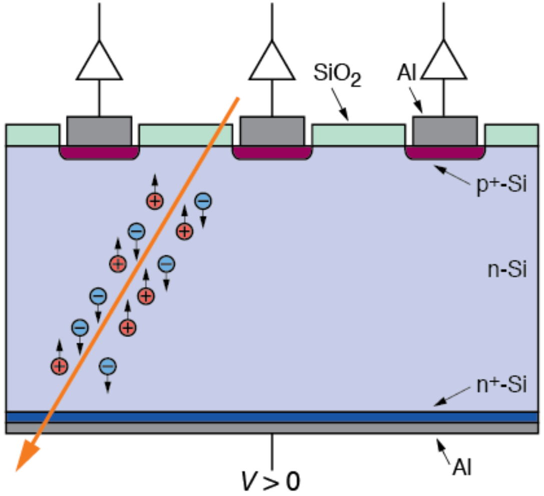
$\leq 10\ \mu m$

precision timing -

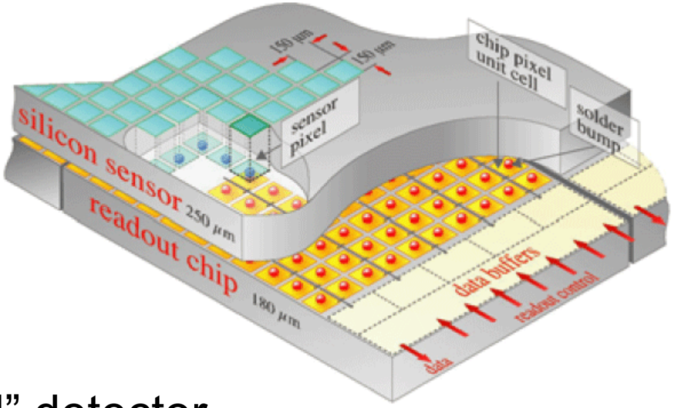
measuring time of arrival before calorimetry

~ 25-40 ps

Silicon sensors used for tracking



Position resolution determined by pixel size, number of pixels hit and the ability for the cluster charge to be shared among pixels



Traditional CMS tracking “hybrid” detector

sensor collects charge from minimum ionizing particles, separate readout chip bump bonded to amplify/digitize signals

CMS silicon inner tracking detector

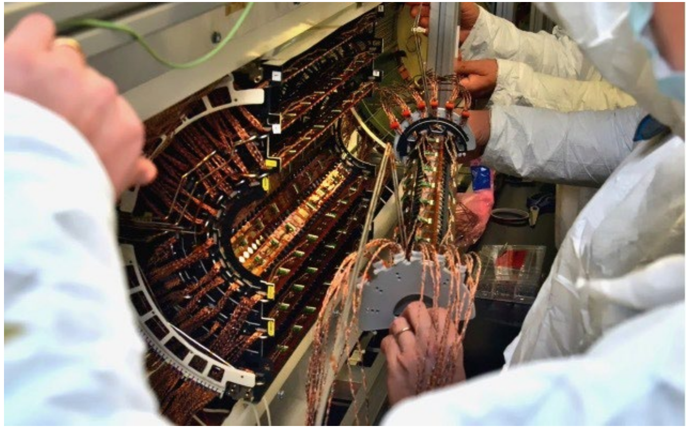
Current detector installed in 2017:

124 Million 100×150 μm^2 pixels

Measures positions of tracks to:

~10μm precision

starting at 3cm from beam

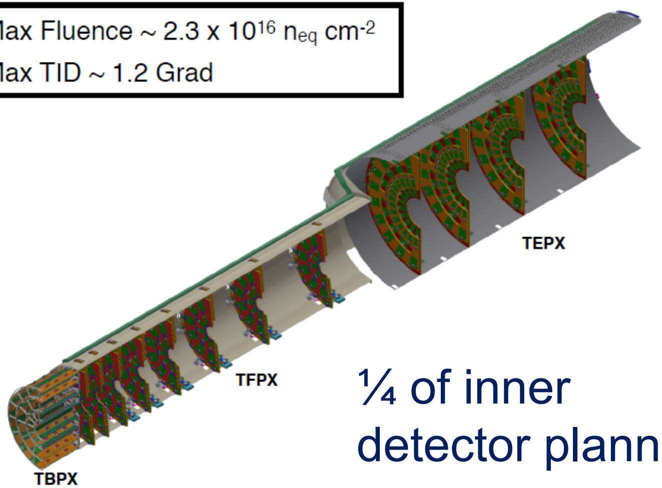


Max Fluence ~ 2.3 x 10^{16} n_{eq} cm^{-2}

Max TID ~ 1.2 Grad

HL-LHC detector to be installed in 2028:

2 Billion 100 x 25 μm^2 pixels



Will be used to disentangle tracks multiple interactions

¼ of inner detector planned

Challenges

- POWER
- Data Rates
- Radiation
- Amount of Material
- Getting signals in and out
- CAN YOU BUILD IT?

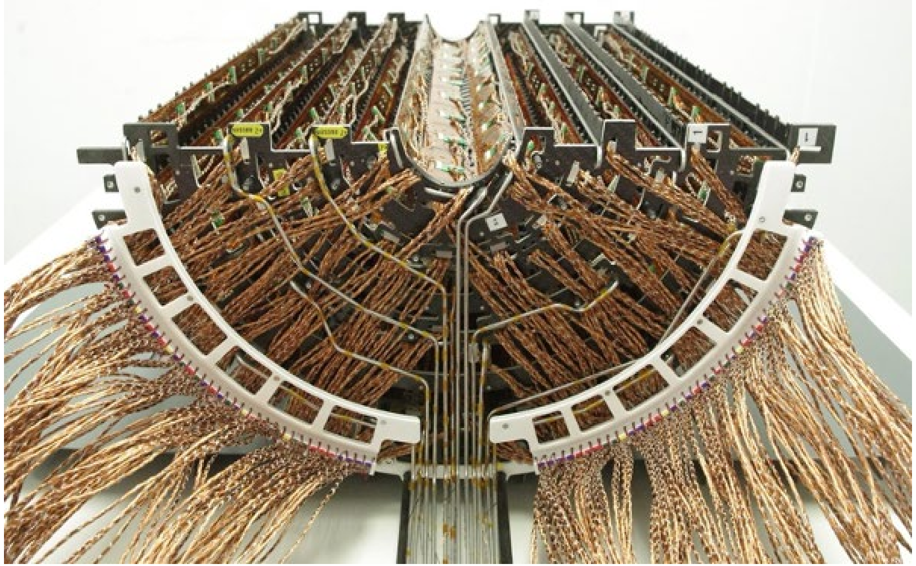
Challenges

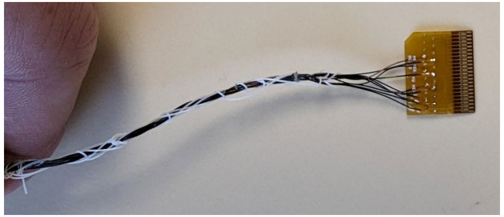
- POWER
  50-60kW with 40-50kA@ 1.2V
- Data Rate   collisions at 40MHz
  operate readout chips @ 1.28 Gbps
  transmit off detector with 5-10 Gbps fibers
- Radiation   particle rate 3 GHz/cm^2
  $\sim 1 \times 10^{16}$ N/cm^2 by end of run

Challenges

- POWER
- Data Rates
- Radiation
- Amount of Material
- Getting signals in and out

CMS Phase I Barrel pixel detector





The 36 AWG twisted pair e-link cables used to get signals out for HL-LHC detector at 1.28 Gbps are hard to build, have mass, and are hard to route!

Challenges

CAN YOU BUILD IT?

CMS HL-LHC inner tracker

Yes! We think we can build it!

What about the next/better tracker?

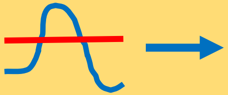
Can you build it?

Need to reduce data at source for next generation detector

Information flow now

On Detector

Keep only pixels with charge above threshold, digitize



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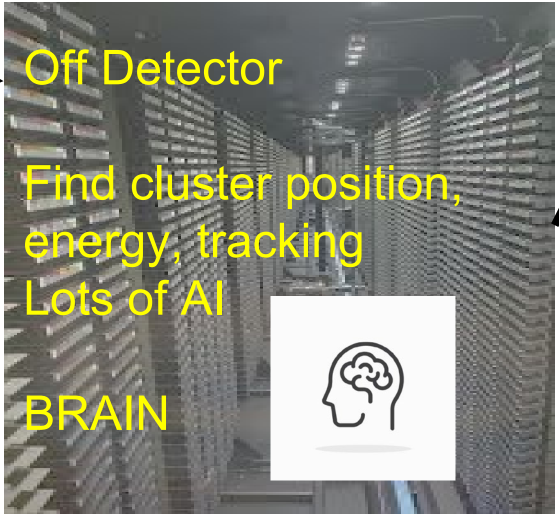
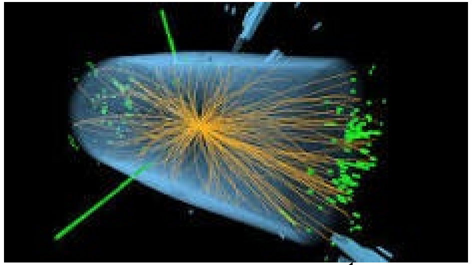
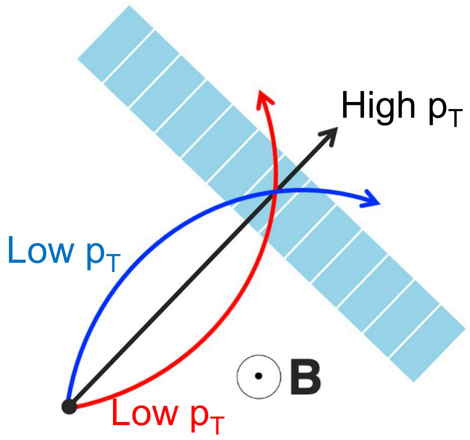
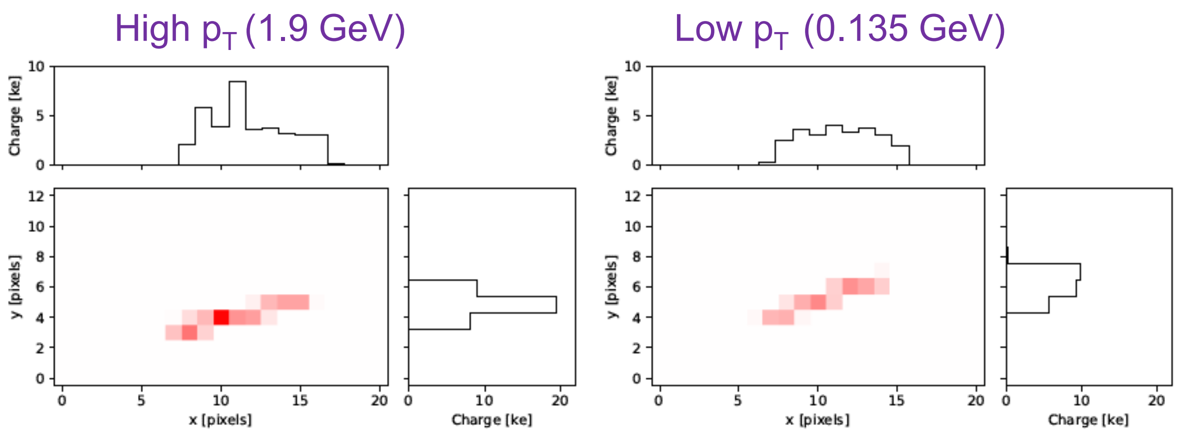
Pixel x,y,E





Smart Pixel Project -reduce data at source



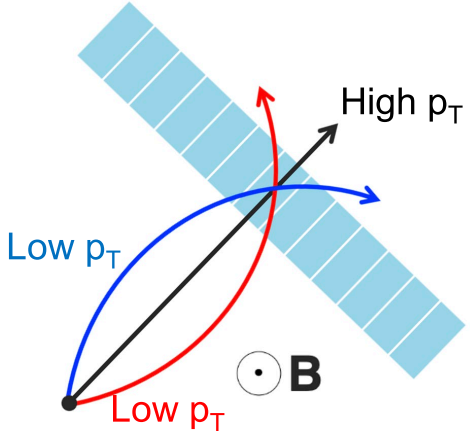


Application for **after** HL-LHC pixel detector

Use ASIC for filtering out pixel clusters with $p_T \leq 0.2$ GeV

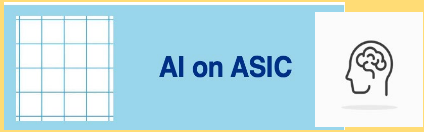
Smaller Pixels are 12.5 × 50 μm

Smart Pixel Project -reduce data at source

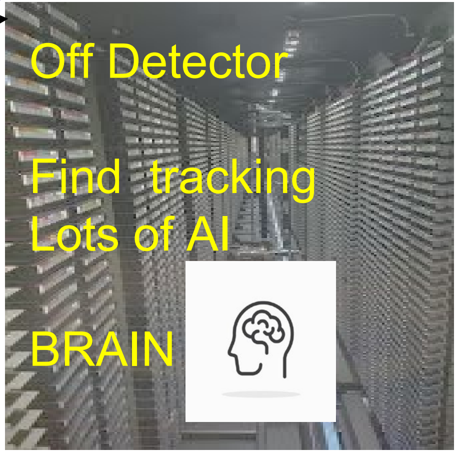


On Detector

Keep only pixels in clusters with $p_T \geq 0.2$ GeV



Pixel x,y, cluster η, ϕ, E

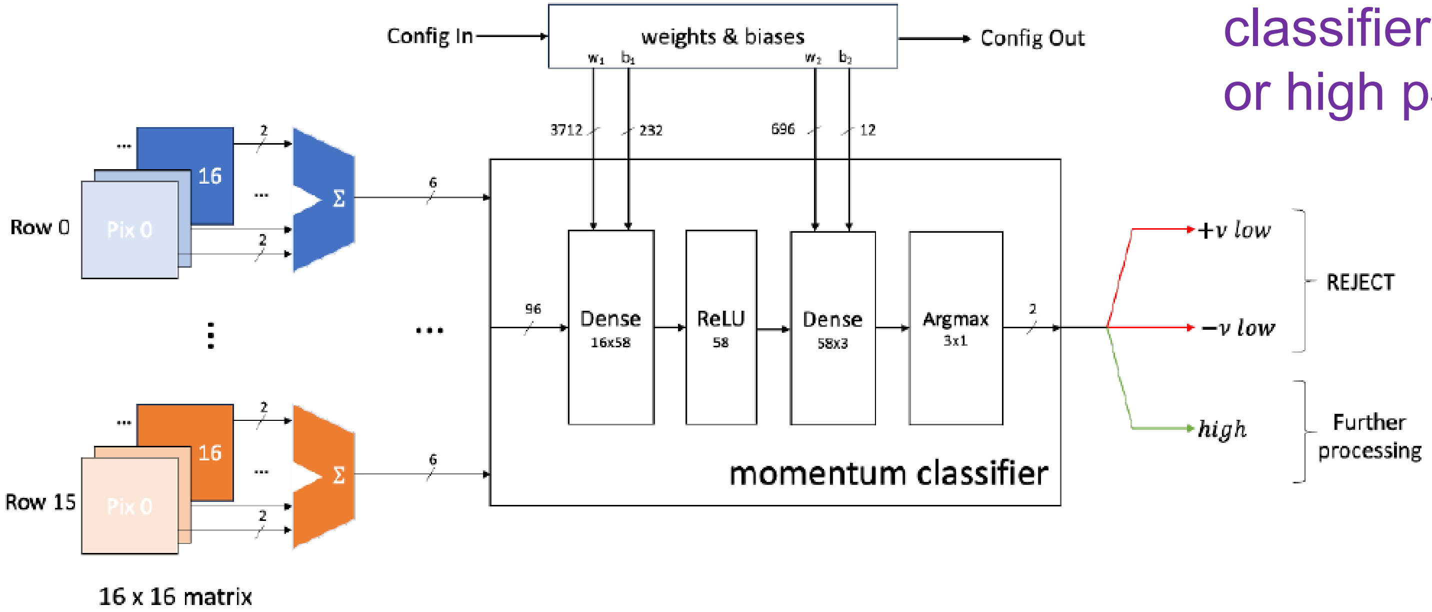


Application for after HL-LHC pixel detector

Use ASIC for filtering out pixel clusters with $p_T \leq 0.2$ GeV

Pixels are 12.5×50 μm

Conventional Neural Network



Output is classifier of low or high p_T

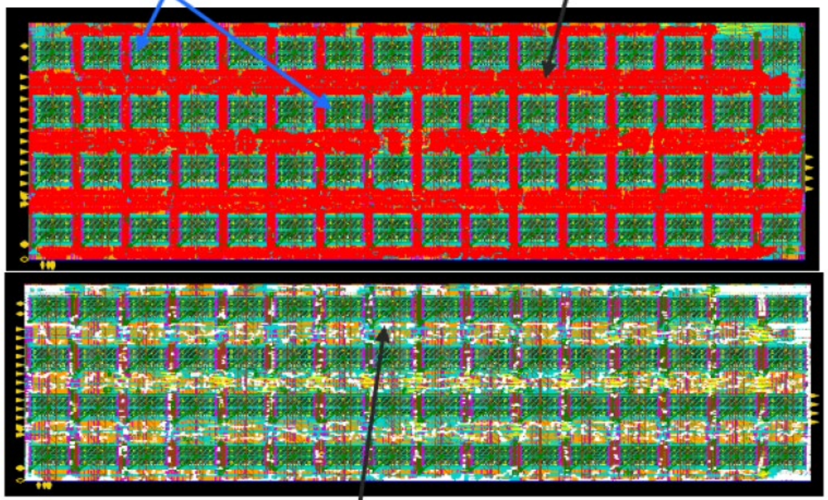
Smart pixel approach

First project: Implement
Classification neural network on chip:

- Use neural network with reprogrammable weights
- 28nm chip layout for 16x16 pixel array

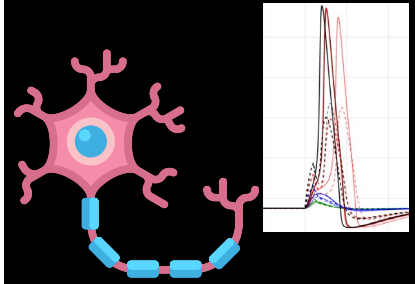
Next → 3D sensor+chip together

Also look at Spiking Neural Network (SNN) implementation



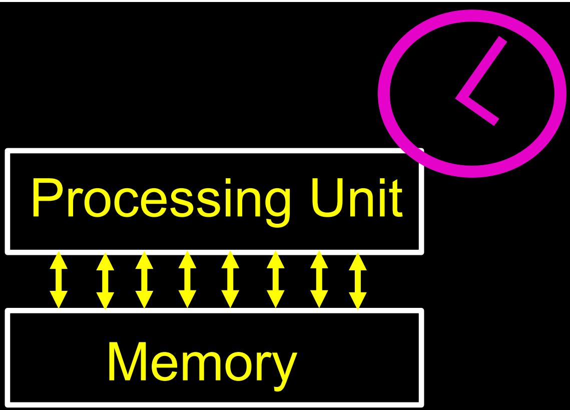
Neuromorphic Computing

~20 watts



Neurons process and store information as needed

Lots of watts



-Processing and Memory Separated
-Clocked data uses lots of power

Dynamic Vision Systems

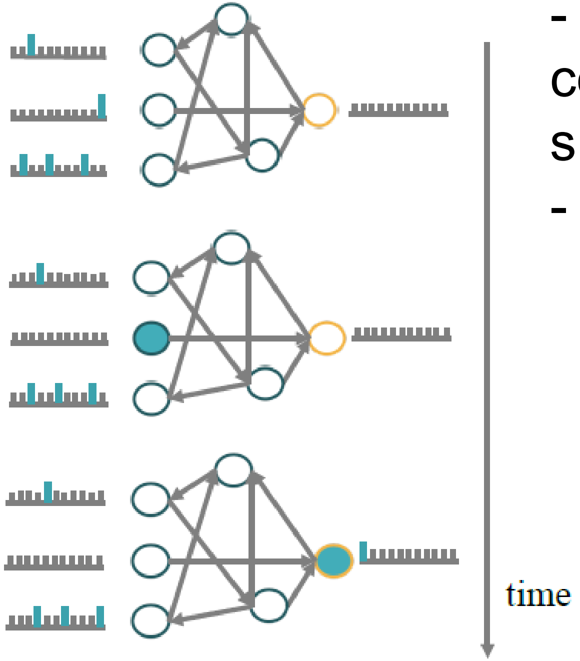
Applications which use Neuromorphic Computing techniques today
These are event based or asynchronous images which only respond to changed pixels in images similar to how human eye works

They use less power can capture faster frame rates than conventional image processors

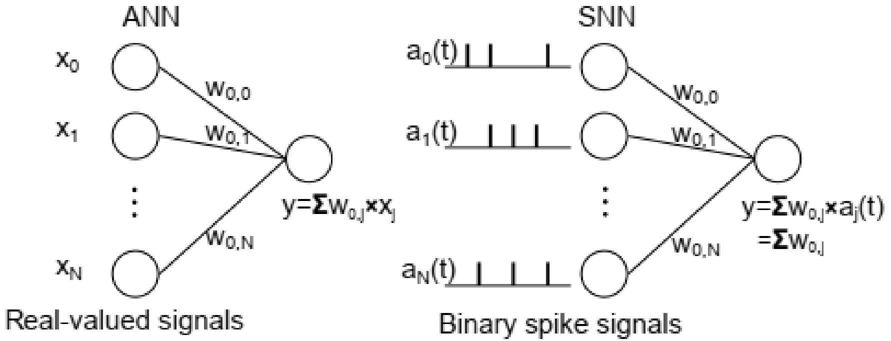
See: talk by Christoph Posch at https://indico.cern.ch/event/1245654
Founded Prophesee systems can process 10K fps, with <10mW (Prophesee.ai)

Spiking Neural Networks (SNN)

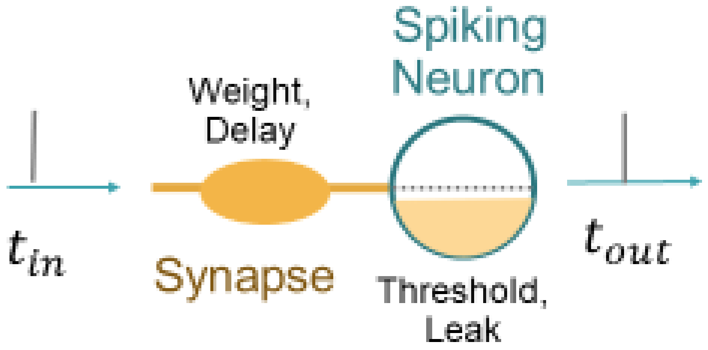
Spiking Neural Networks



- Data spikes excite “neurons” which communicate via synapses by transmitting spikes
- Use temporal information



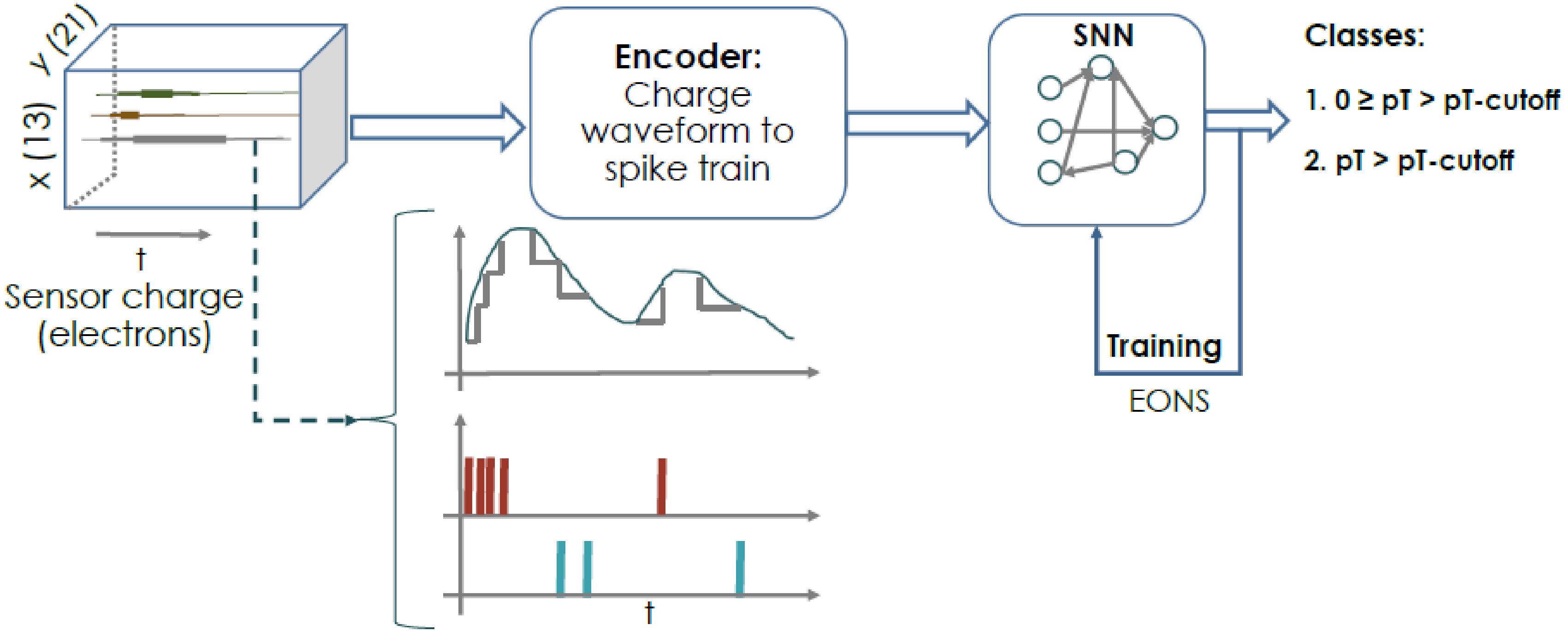
Neuromorphic Computing – Basic Model of Operation



- Inherent temporal dynamics
- Neuron fires with charge exceeding threshold – **Leaky Integrate and Fire**
- Multiple tunable parameters
  - Synaptic weights, delays
  - Neuronal thresholds, leaks
  - Network architecture

Oak Ridge National Lab has implemented models of these neurons and synapses in FPGA systems for radiation monitoring that use very little power

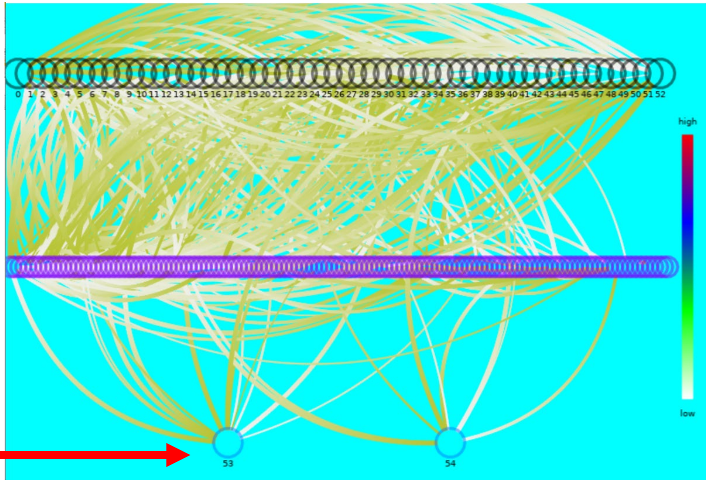
Smart pixel SNN implementation



Results of SNN trained classifier for Smart Pixels

Models	DNN	DNN (quantized)	SNN (this work)
Signal Efficiency	94.8 %	91.7 %	**91.89%**
Data Reduction	24.02 %	25.71 %	**25.47%**
Neurons	128	128	**84**
Parameters	2049	2561	**930**

- Use Network with highest signal efficiency for p_T> 2.0GeV clusters
  - Trained Network size: 84 neurons, 493 synapses

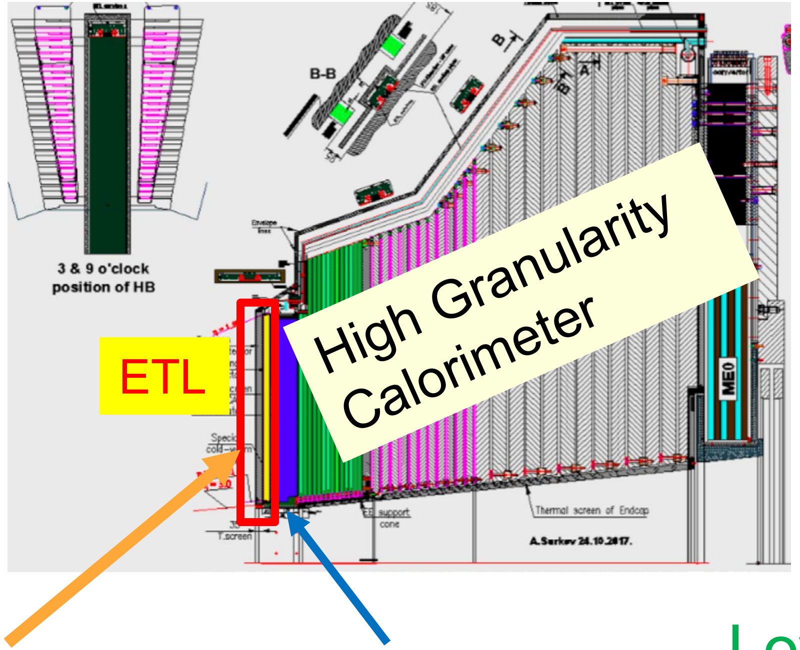


2 output neurons that fire depending on which of the two classes

Can we use SNNs for data reduction for high precision position and timing detectors?

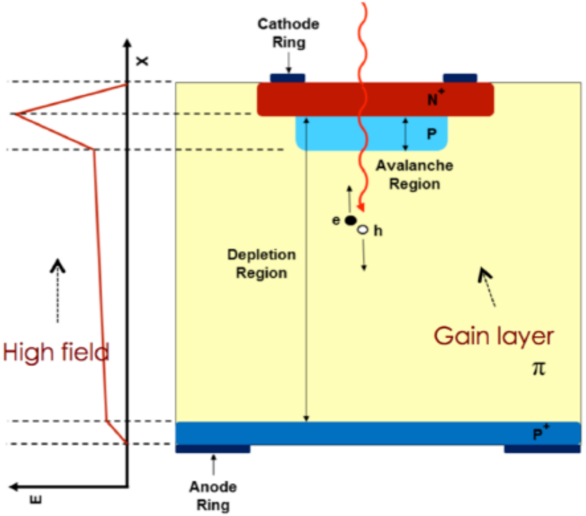
Precision Timing with Silicon Detectors

CMS HL-LHC Endcap Timing Layer



Interaction point
~1m away

Neutron
moderator



Low Gain Avalanche Diode (LGAD)

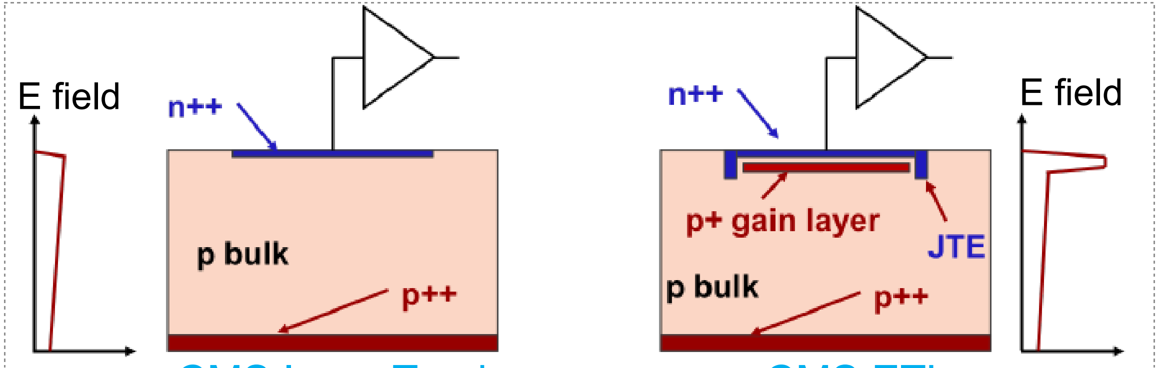
Measure time of track to ~25ps

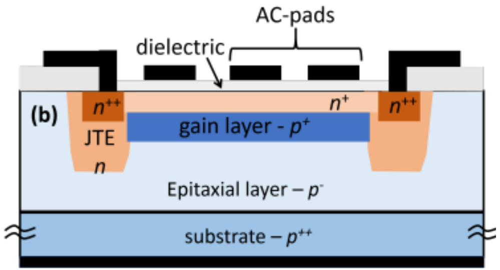
Challenges

- Electronics readout chip and readout system need to be carefully designed to obtain timing precision
    - currently 25 ps for CMS ETL
- Little charge sharing among pixels with current LGAD design
    - position resolution limited by pixel size
        ~1.3mm x 1.3mm

Timing information with Low Gain Avalanche Diode (LGAD) detectors

Traditional Silicon Detector | **Ultra Fast LGAD** | **AC coupled LGAD**

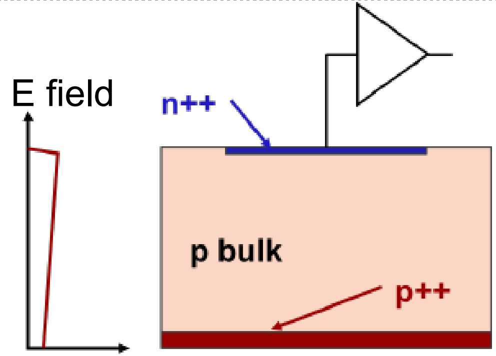




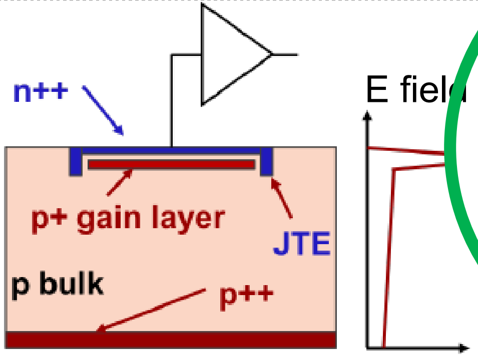
	CMS Inner Tracker	CMS ETL	?
<u>Substrate</u>	need sufficient thickness	thin but limited acceptance due to segmentation	thin no acceptance limit
<u>Charge Sharing among pixels</u>	yes exploited	limited charge sharing due to electrode size	exploitable thanks to small electrode
Position resolution	~3-10μm	~50-300μm	1-100μm?
Timing resolution	~ns	~20-40 ps	20-40ps?

Timing information with Low Gain Avalanche Diode (LGAD) detectors

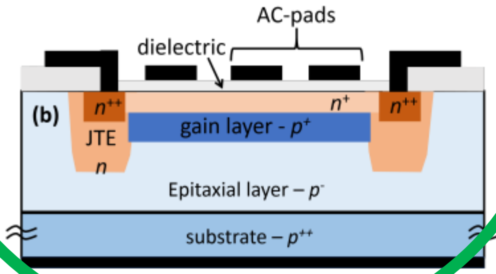
Traditional Silicon Detector



Ultra Fast LGAD



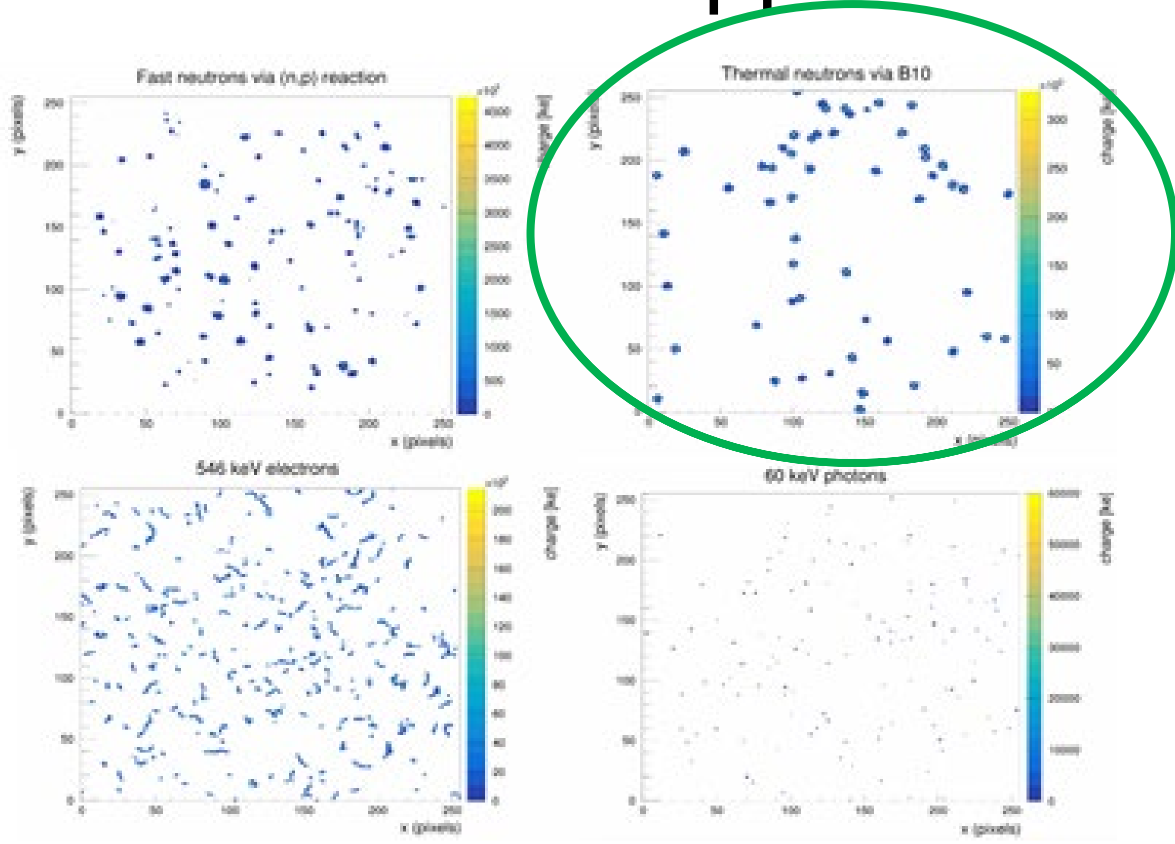
AC coupled LGAD



	Traditional Silicon Detector	Ultra Fast LGAD	AC coupled LGAD
	CMS Inner Tracker	CMS ETL	?
Substrate	need sufficient thickness	thin but limited acceptance due to segmentation	thin no acceptance limit
Charge Sharing among pixels	yes exploited	limited charge sharing due to electrode size	exploitable thanks to small electrode
Position resolution	~3-10μm	~50-300μm	1-100μm?
Timing resolution	~ns	~20-40 ps	20-40ps?

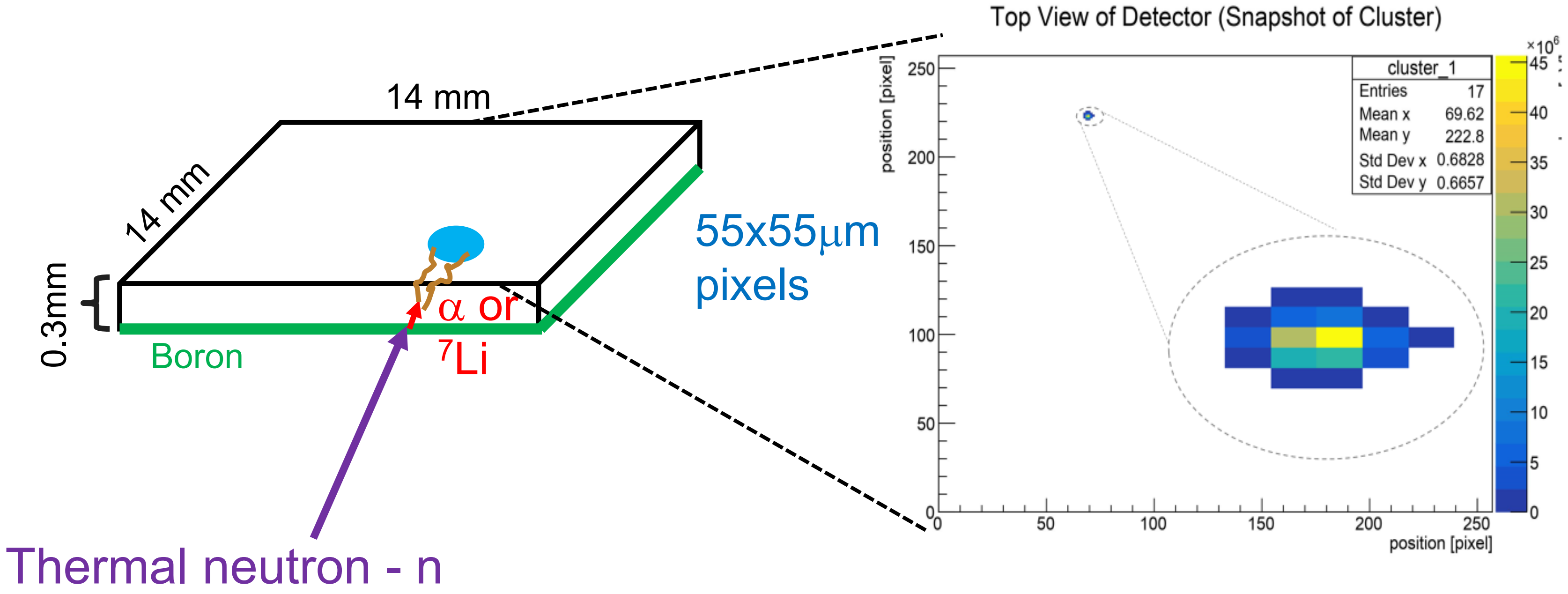
Neutron Beam monitor application

- Thermal neutrons interact with ^{10}B. Large clusters form from plasma charge effect
- Needs precision timing and tracking
- Eventually will use AC coupled LGAD detectors



Neutron Beam Monitor Application

First start with traditional silicon simulation

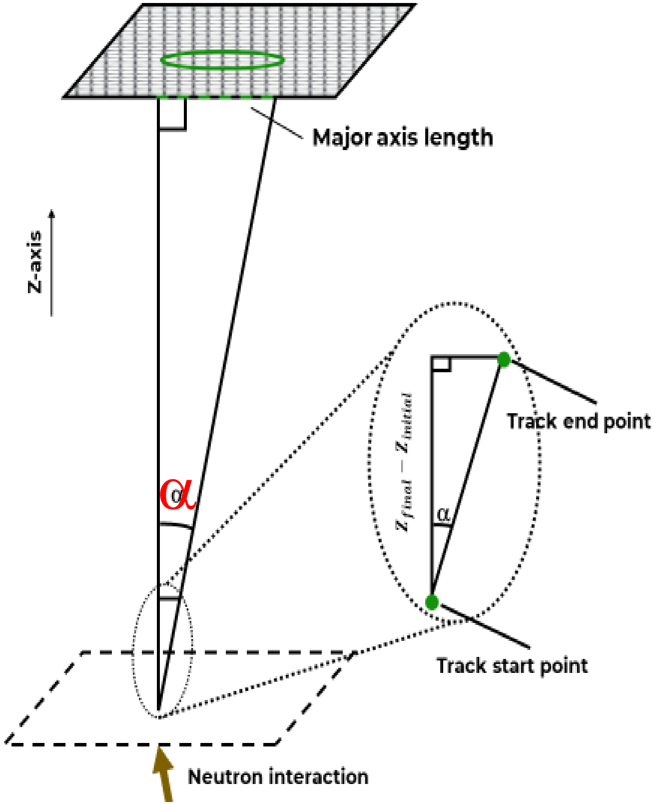


$$^{10}B + n \begin{cases} \rightarrow \alpha_1^*(1.47MeV) + {}^7Li^* \ (0.84\,\mathbf{M}eV) + \gamma \\ \rightarrow \alpha_0(1.78MeV) + {}^7Li(1.01MeV) \end{cases}$$

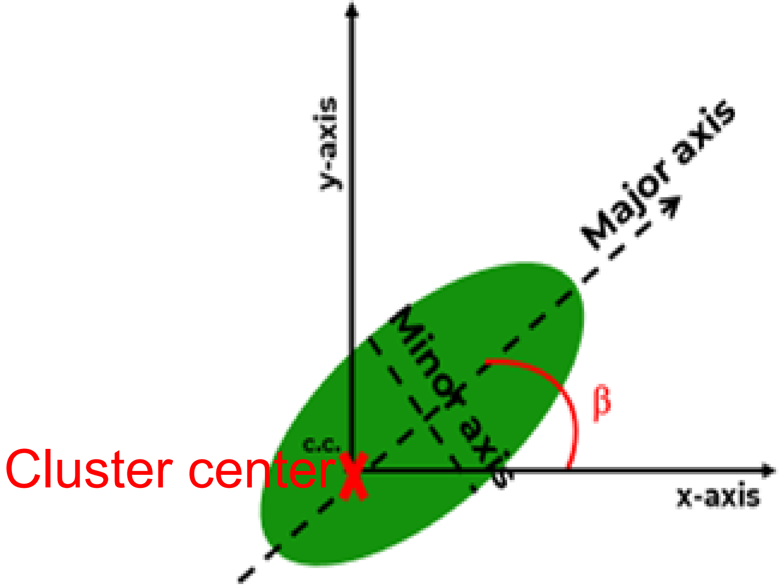
Size of cluster ~35 pixels

GOAL to measure cluster/track information:

center position (x,y) Energy (E), angles of incidence (α,β)

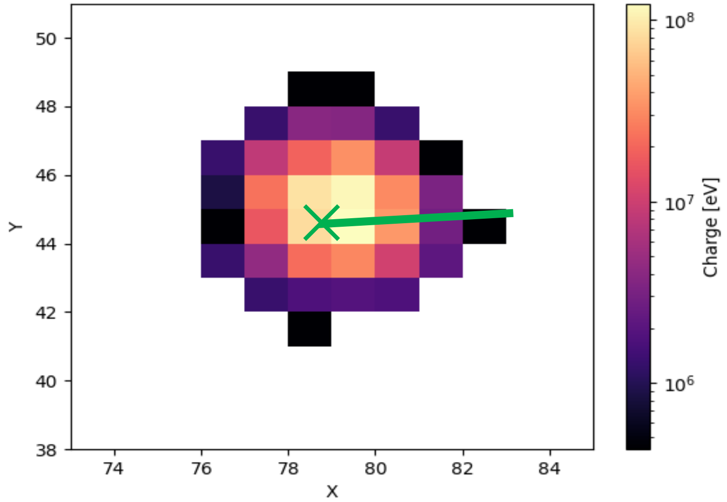


2D Top View of Detector



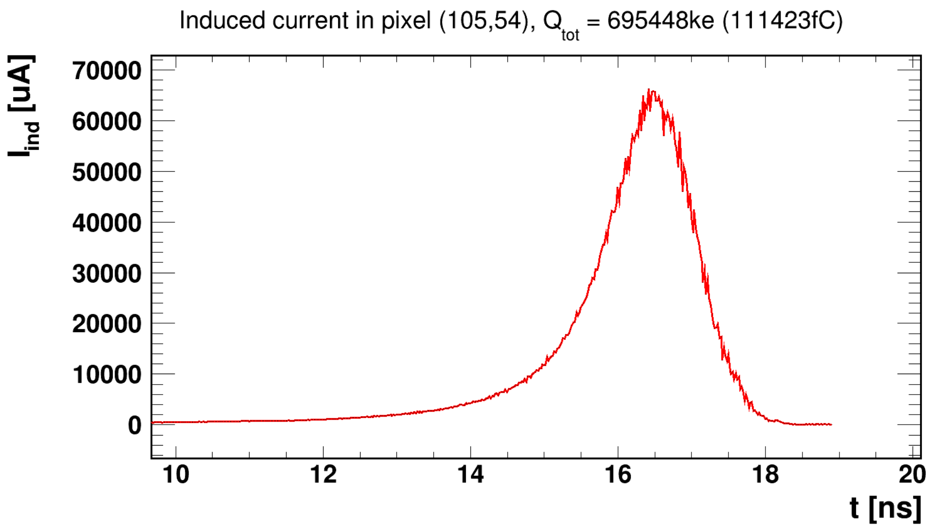
First steps

- Use traditional silicon detector (not LGAD) to start
  55×55μm pixels in 0.3mm thick detector
- Use Timepix4 ASIC for readout
  can use time-over-threshold,
  time of Amplitude (<200ps) with
  16 bit counter, ~800e threshold,
  3.6MHz/mm^2/s hit rate capability
- Simulate events with Allpix2 software
  (https://allpix-squared.docs.cern.ch/)
  Has model for Timepix output already included
- Calculate Offline x_c, y_c, E, α, β and compare with
  truth information to measure resolution



res (x_c, y_c) ~1μm

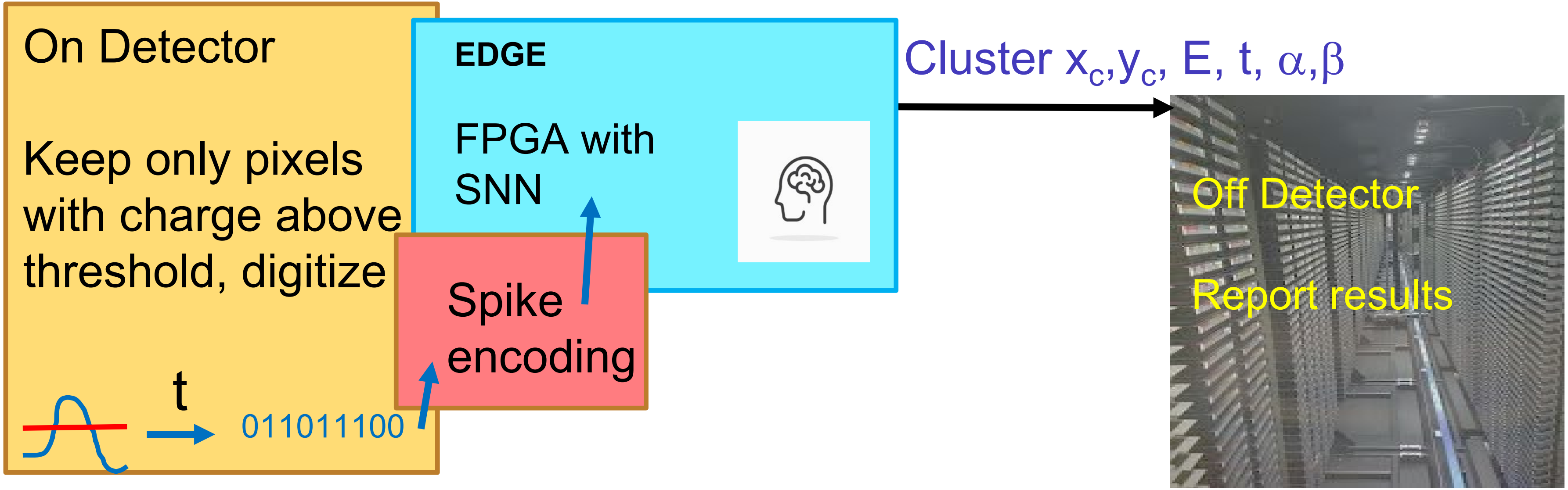
Next Steps



- Put time characteristics into simulation

  Implement detailed model of charge multiplication, electrostatic repulsion (plasma effect), electric field (using TCAD) in MC Charge transport code (Allpix^2) and output
- Study encoding for SNN
- Train SNN to output regression variables
- Implement SNN in FPGA

Start with SNN implementation on FPGA



SNN with Digital stream pipeline maps well to FPGA
Has low latency for sparse data
DNNs are harder to implement on FPGAs

Later SNN implementation ASIC

On Detector

Dream for full SNN analysis of cluster information with ASIC

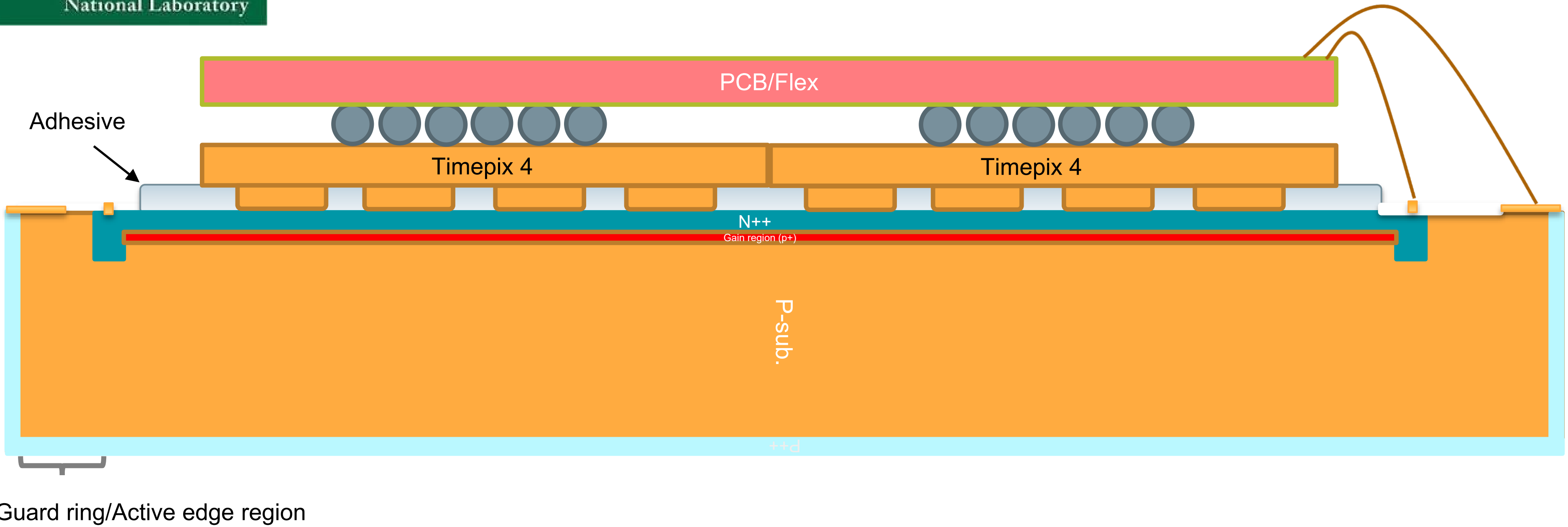
Cluster x_c, y_c, E, t, α, β

Big issue: Spike Encoding implementation at speed

Challenges

CAN YOU BUILD IT?

M. Benoit Proposal



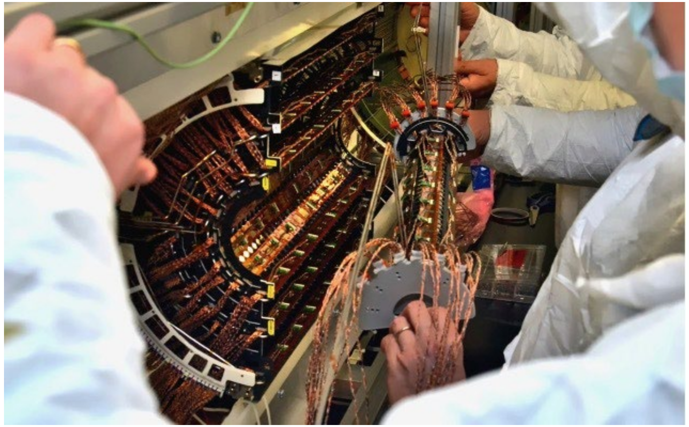
Can achieve capacitive coupling and transmit signal with good efficiency via a thin adhesive layer

- **No electrode required** on the AC-LGAD side, making it a simpler structure to manufacture.
- AC Coupling can be achieved via a combination of **thin oxide-adhesive layer, ENIG pads from ACF experience**
- **No complex interconnect** method necessary, no lithography
- Multiple ASICs can be tiled on a **large area AC-LGAD**
- **Large charge deposition and multiplication provide spatial amplification**

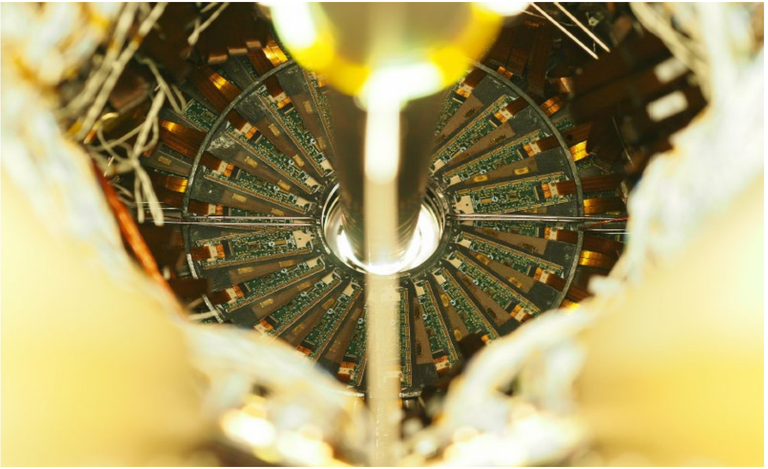
Summary

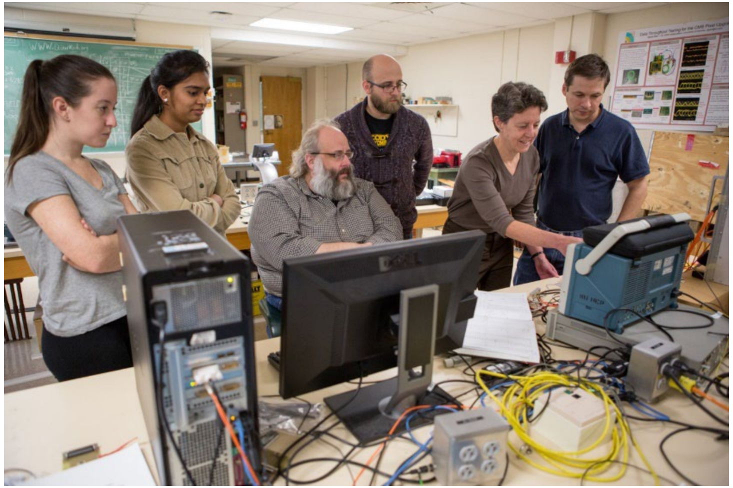
- Dreams of particle detectors with precise position and time resolution have to confront how to reduce the data output from the detector
- Lots of work now in implementing AI on ASICs for particle tracking applications
- Many technical hurdles are being overcome
- There is a pathway to implementing SNNs on the detector

BACKUP



CMS inner detector installed in 2016 built partially at KU

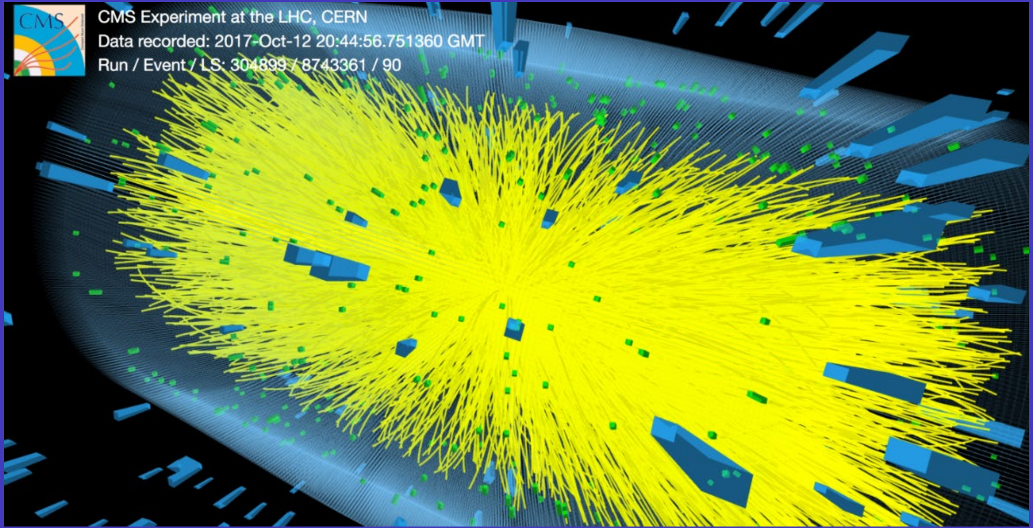




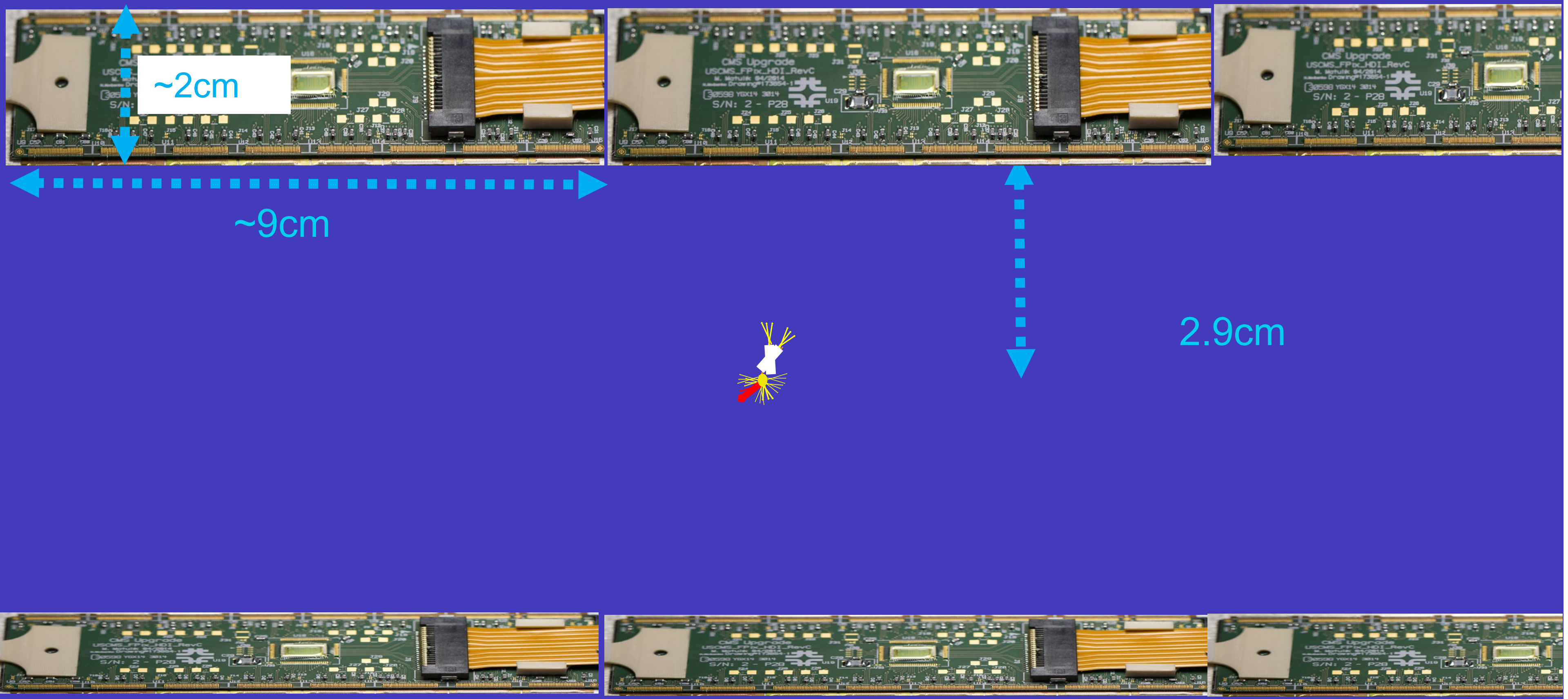
Build detectors that track particle trajectories

Current CMS inner tracking detector

- made from silicon
- includes 124 million pixels
- measures positions with resolution ~10μm



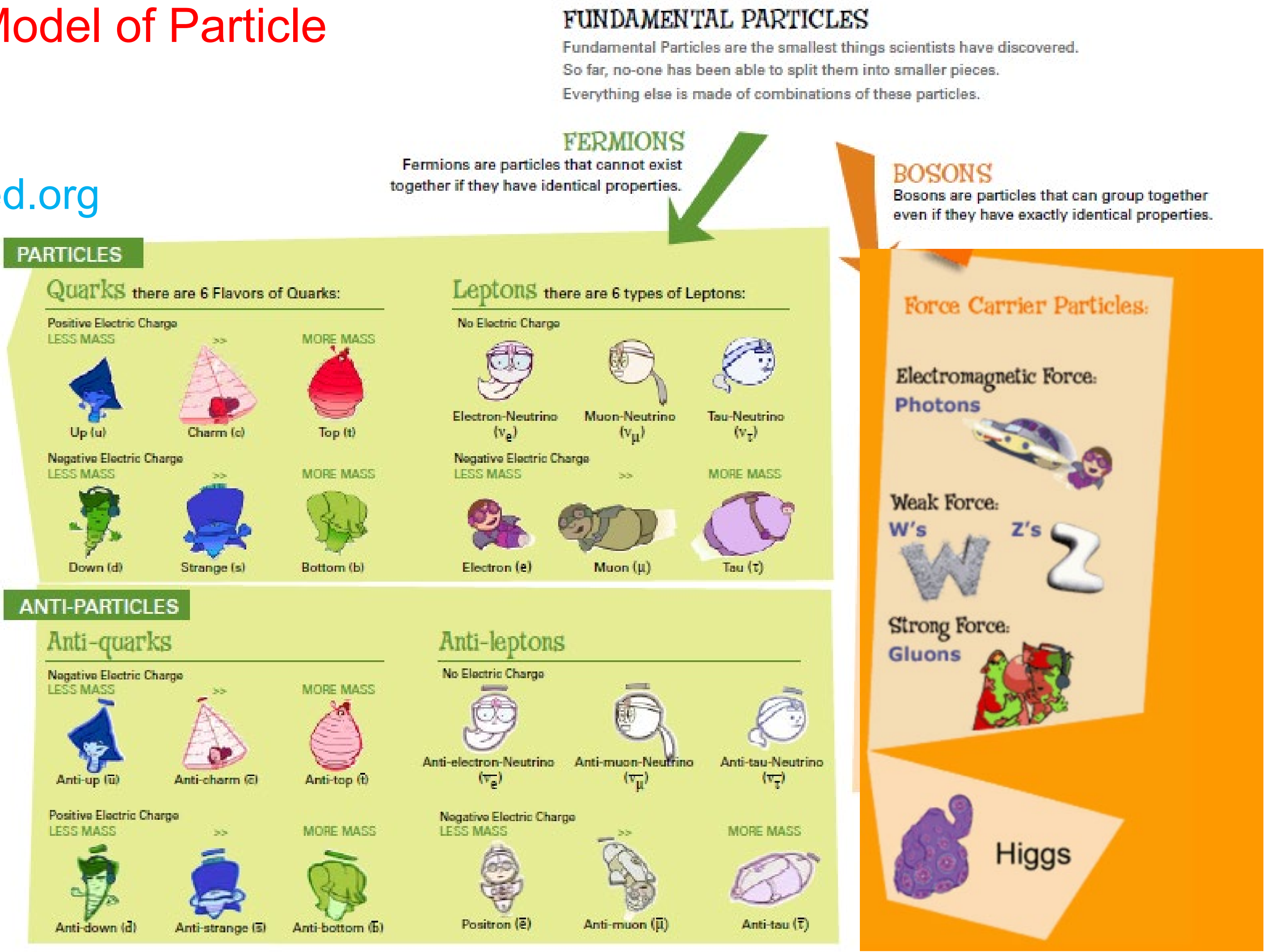
They then travel to detector



Zoom out some more - this shows part of the first layer of detectors

Standard Model of Particle Physics

www.quarked.org

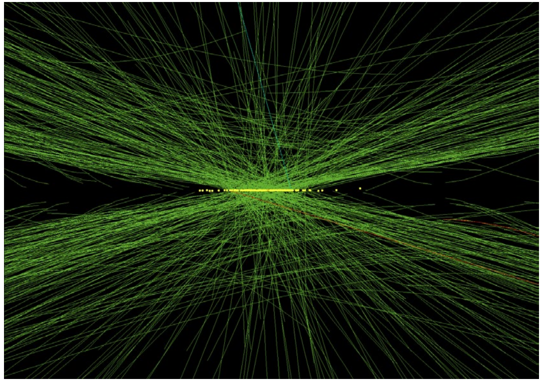


Calculate Offline x_c, y_c, E, α, β

Getting more data implies improving tracking detector

- New detector being built to start taking data in 2029
- Electronics supports taking 40 Million snapshots/second with up to 200 collisions expected per snapshot

Now



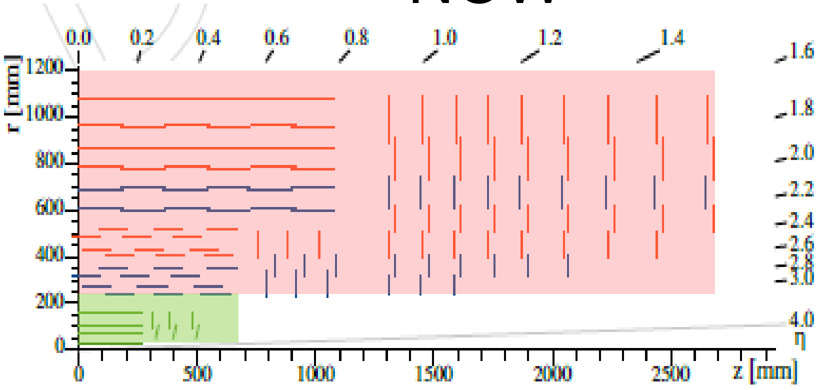
Simulation of expected snapshot with new detector

Need: Radiation tolerance, Increased Granularity, Robust Pattern Recognition

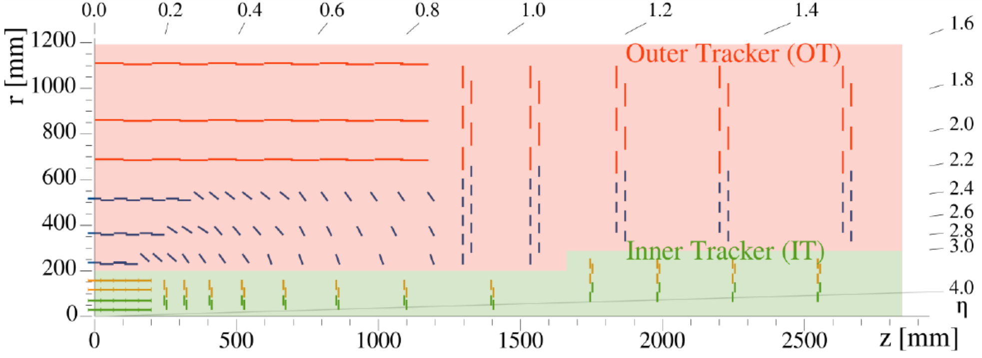
Design of HL-LHC CMS tracking detector

Tracking Detectors

NOW



Proposed HL-LHC



1/4th of total tracker

Both have Inner pixel detector with Outer silicon strips

Bigger differences include:

Inner pixel detector has 124M channels → Inner pixel tracker has 2B channels!

No trigger information

Outer tracker has L1 trigger modules

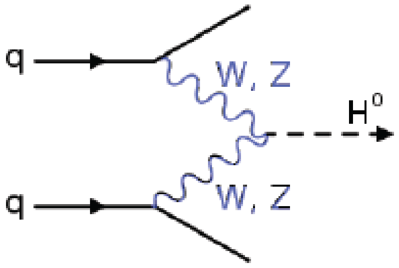
Some Physics Goals

1. Study the SM Higgs

Vector Boson Fusion production important

need forward jets and leptons

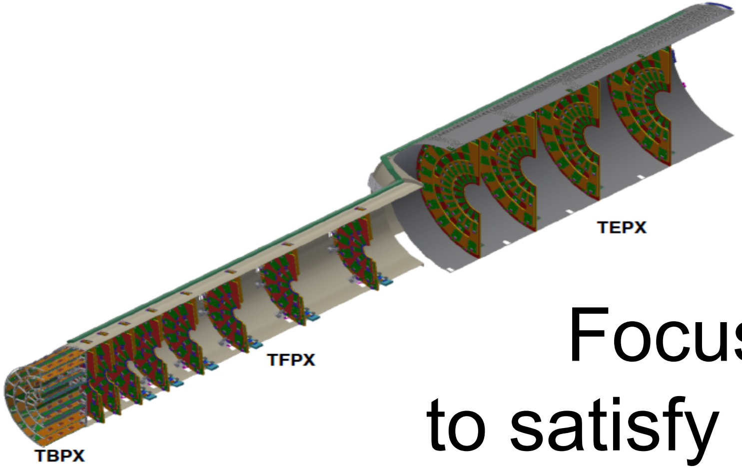
Higgs Production via Vector Boson Fusion



2. Look for Beyond Standard Model physics

Need good mass resolution:

Improved 2-track separation, Reduced material in tracking volume



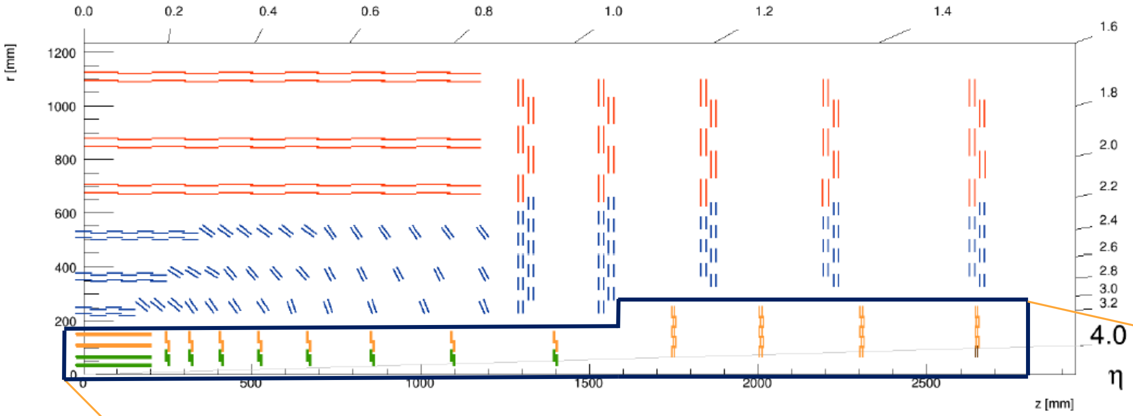
Focus here: Inner Tracker to satisfy most of the requirements

Requirements,

- Contribution to the level-1 trigger – from outer tracker
- Increased granularity
- Improved two-track separation
- Robust pattern recognition
- Extended tracking acceptance in η
- Radiation Tolerance
- Reduced material in tracking volume

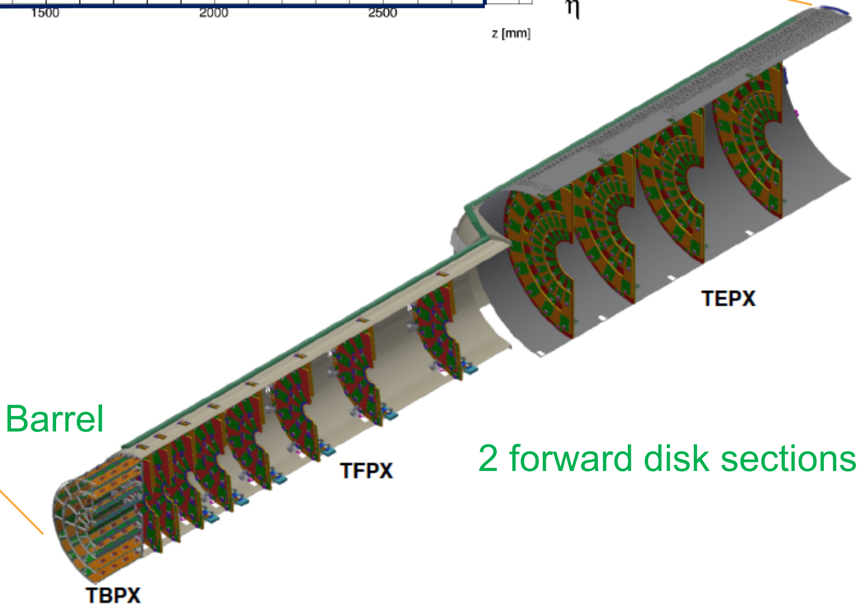
- Large channel count
- Smaller pixel size (by factor of 6) $100 \times 25\ \mu m^2$
- More forward detectors

The CMS Tracker for HL-LHC

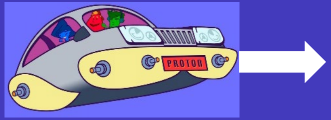


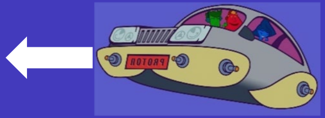
Inner Pixel Tracker

- 4352 modules, 4.9 m^2, 2×10^9 pixels
- Coverage up to |η| of 4.0
- Occupancy < 0.1%
- Hybrid modules with 2 or 4 readout chips
- Mechanics made so it can be removed for maintenance
- Maximum Fluence ~ 2.3×10^{16} n_{eq} cm^{-2}

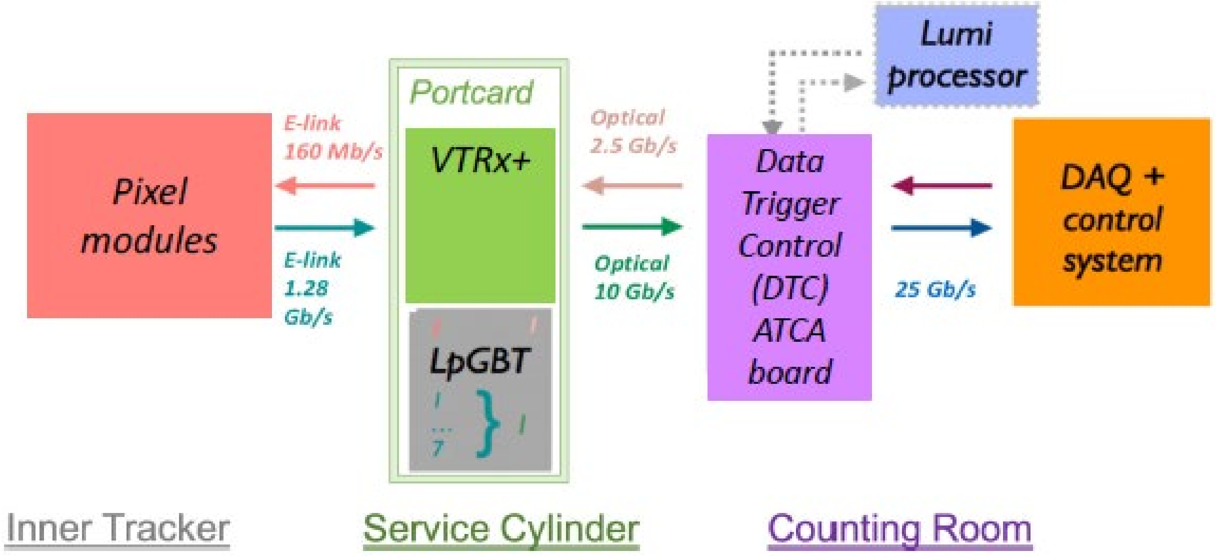


Two Protons collide





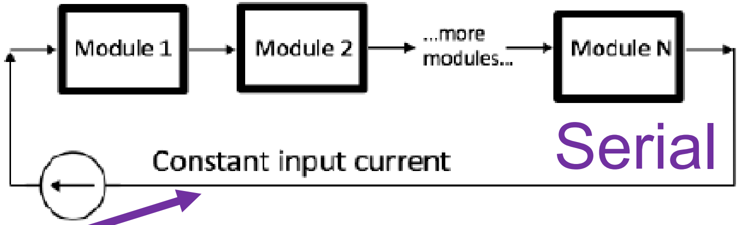
More Challenges



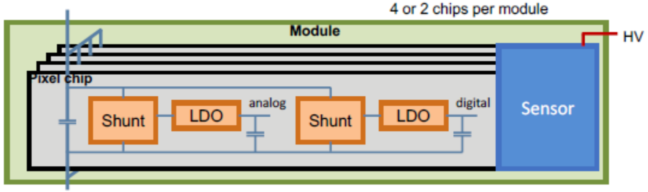
- POWER
- Data Rates
- Materials and getting signals in and out

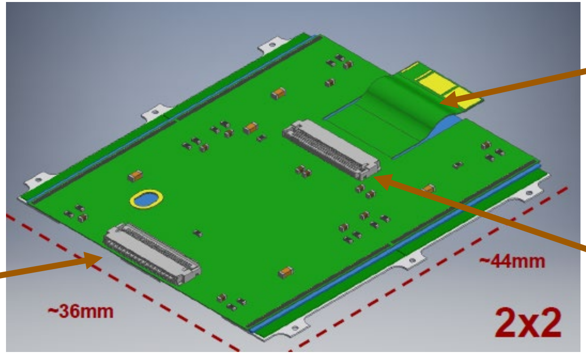
Modules and Powering

- Enormous power budget
  50-60kW with 40-50kA @ ~1.2V
- Problems with direct powering
  too much material required
- Problems with local conversion
  - DCDC converter radiation hardness
  - space limitations
- Pixel Readout chip is only active electronics on Module High Density Interconnect (HDI)



Serial Powering





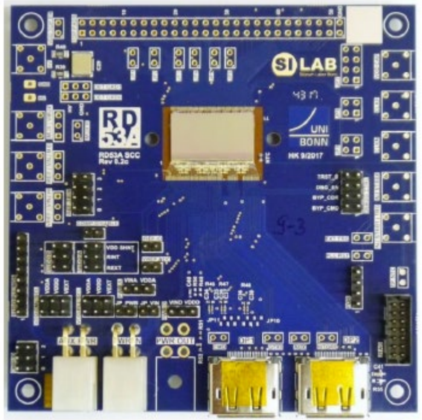
Power input pigtail

I/O connector for e-link

Power output connector

Module HDI design

Readout Chip Development by RD53 Collaboration for ATLAS and CMS



- 65 nm CMOS technology
- 50×50 μm^2 cell
- Low threshold (≤ 1000 e$^-$)
- High Hit and Trigger rate
  - up to 4× 1.28 Gb/s
- Radiation Resistant
- Serial Powering capabilities
- CML Signal Driver
- CMS chip size:
  16.8 × 21.6 mm^2
  336 × 432 cells

NOW:

Chip communicates at

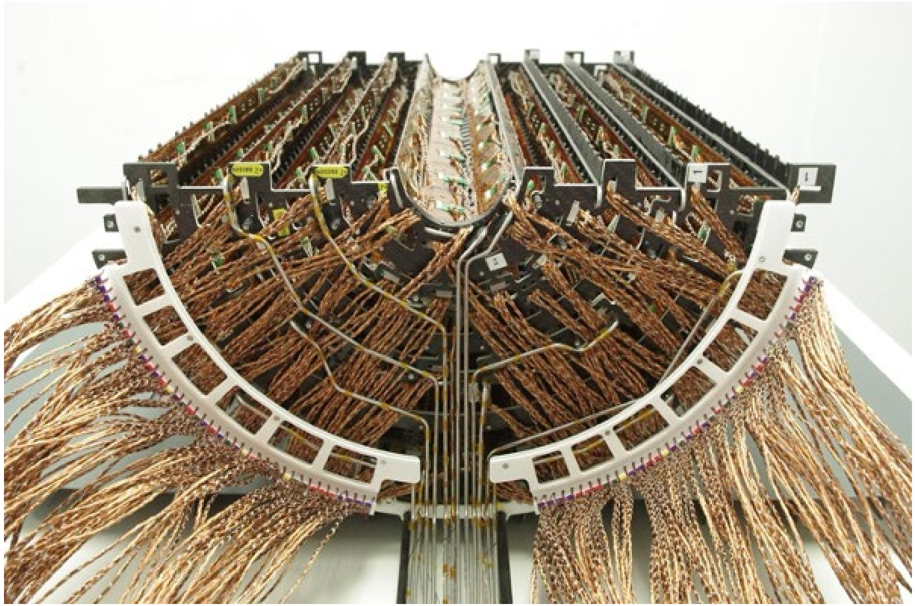
400 Mb/s

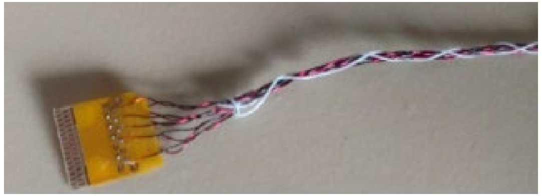
An example – electronic links

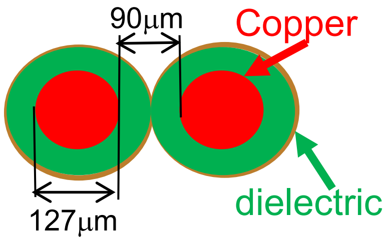
Use differential micro-twisted pairs

Pixel Barrel detector NOW uses 36 AWG twisted pairs

So what's to worry about: 1.28 Gbps







- Need to match 100Ω impedance
- Small wire has big skin losses
- Transmitting signals up to 2m
- Cross talk
- manufacturing
- Fragile construction …

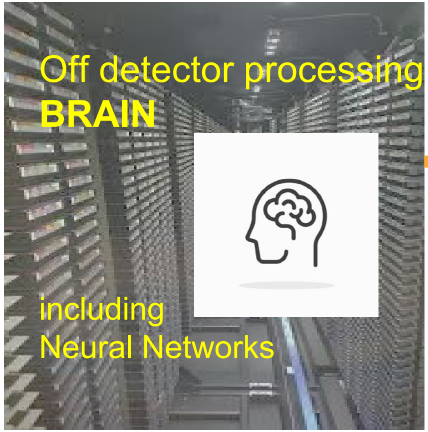
E-links can be built to transmit 1.28 Gbps signals up to ~2m

Building and testing these is non-trivial

What about the future?

Need to move off detector processing onto the detector so not as much data is transported off detector

NOW



FUTURE

Detector in beam

space + time + brain

Use neuromorphic (brain inspired) computing

- Timing/Event driven data
  - Dynamic Vision Sensing
- Spiking Neural networks (SNN)
- Detector needs new sensor electronics/readout chip with SNN embedded

Can improve:

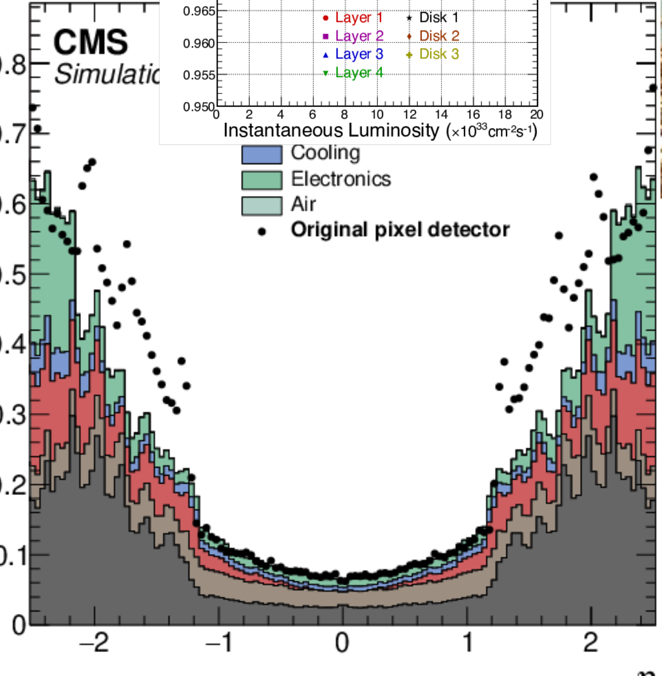
- time and space resolution – incorporating timing information directly
- Energy consumption

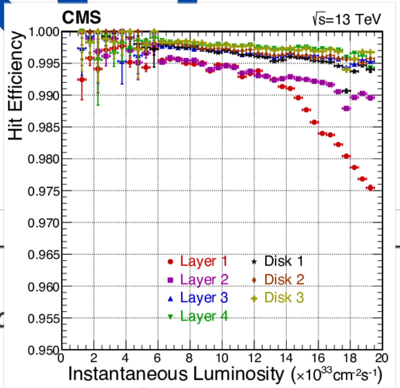
Conclusion

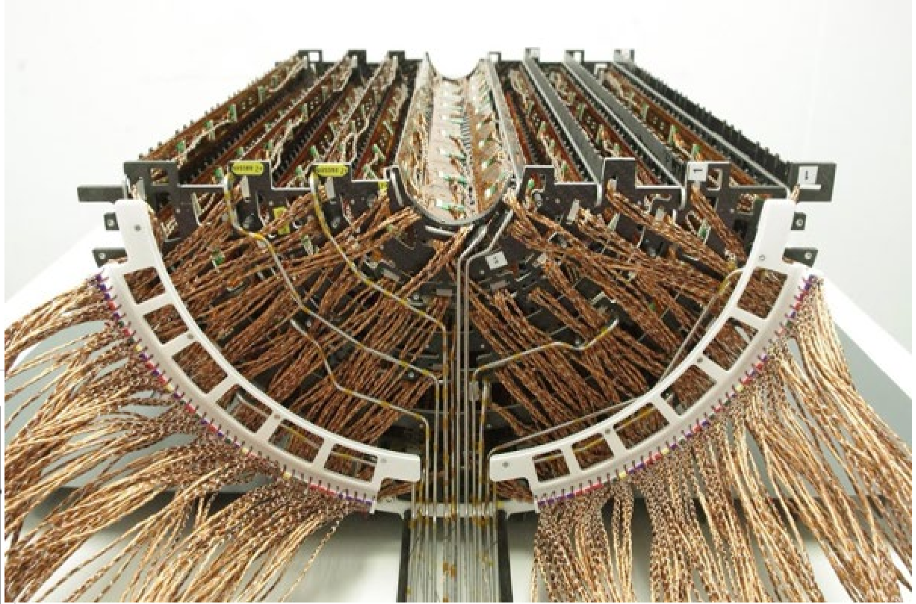
The CMS collaboration
- is taking more data and looking for Beyond Standard Model physics
- is building a new tracking detector for the HL-LHC

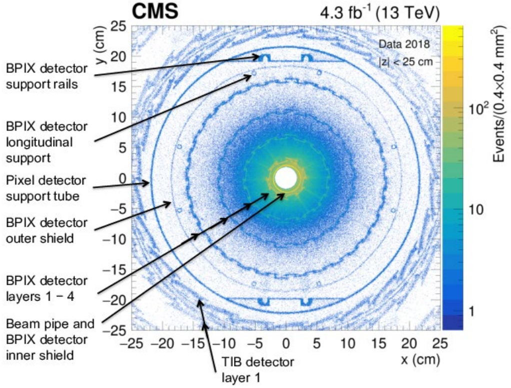
Challenges for building the detector include:
- Power
- Data Rates
- Materials and getting signals in and out

Explored challenges of e-link cables to carry signals

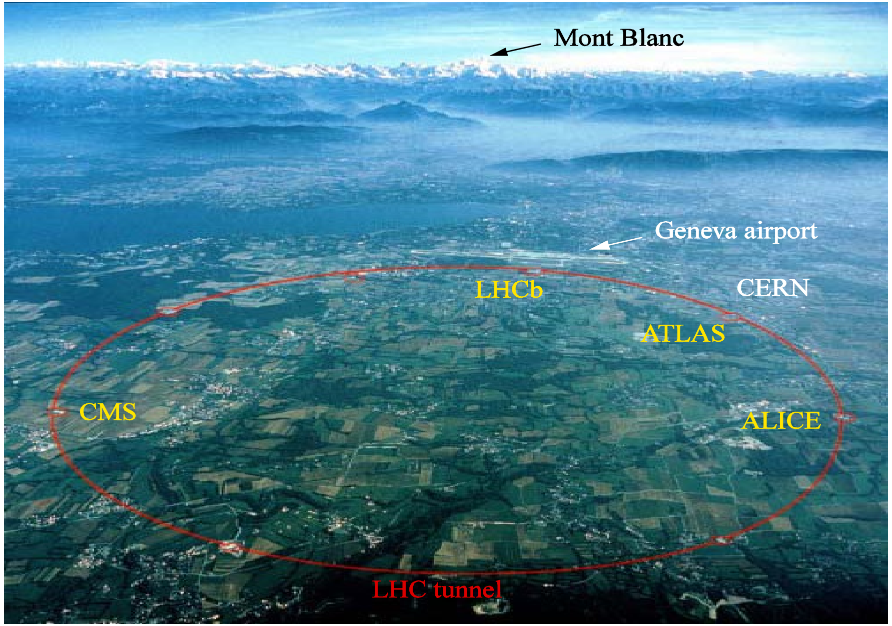

CMS
Simulatio
Cooling
Electronics
Air
Original pixel detector
0
−2
−1
0
1
2

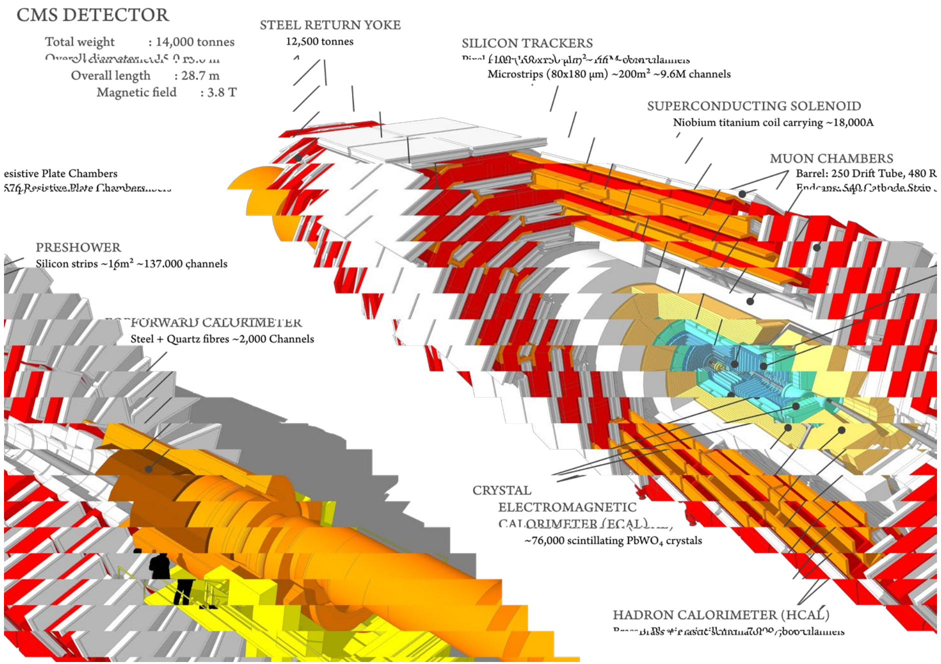

CMS
√s=13 TeV
Hit Efficiency
1.000
0.995
0.990
0.985
0.980
0.975
0.970
0.965
0.960
0.955
0.950
Layer 1
Layer 2
Layer 3
Layer 4
Disk 1
Disk 2
Disk 3
0 2 4 6 8 10 12 14 16 18 20
Instantaneous Luminosity (×10^33 cm^-2 s^-1)

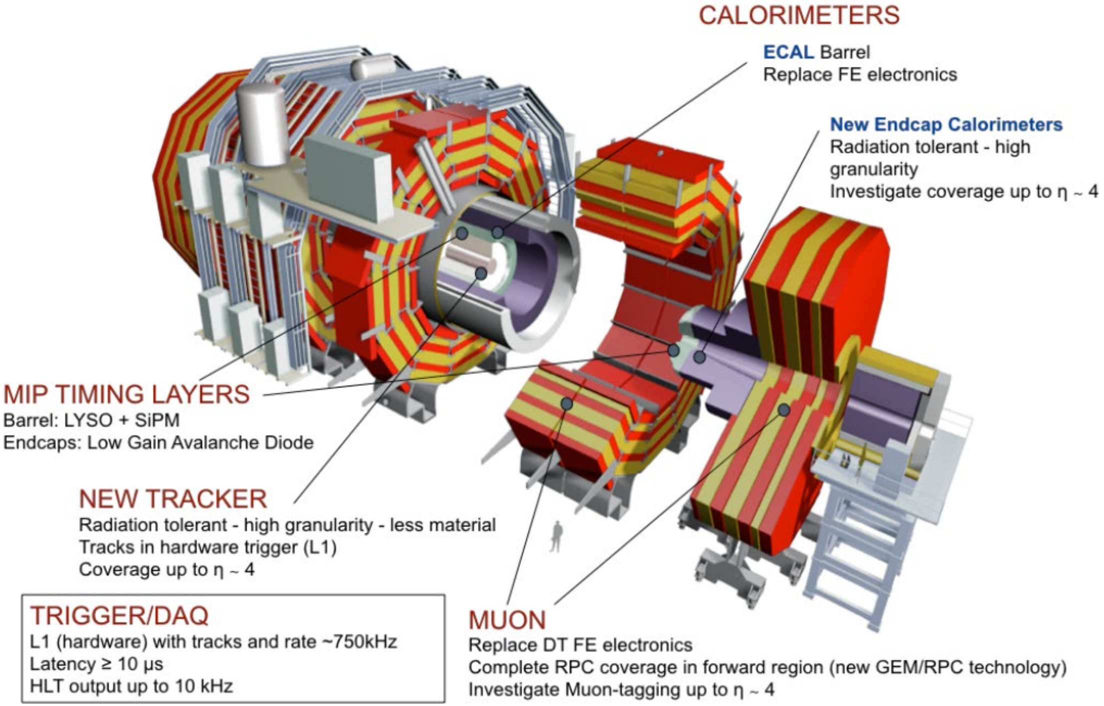



CMS
4.3 fb^-1 (13 TeV)
Data 2018
|z| < 25 cm
y (cm)
x (cm)
Events/(0.4×0.4 mm^2)
BPIX detector support rails
BPIX detector longitudinal support
Pixel detector support tube
BPIX detector outer shield
BPIX detector layers 1 − 4
Beam pipe and BPIX detector inner shield
TIB detector layer 1

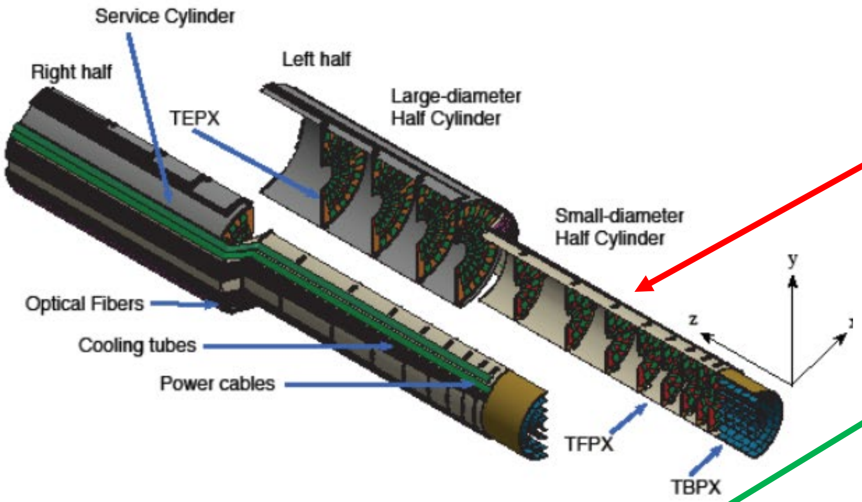
I am part of the CMS collaboration ~3000 physicists
Operate a detector located at the Large Hadron Collider near Geneva, Switzerland

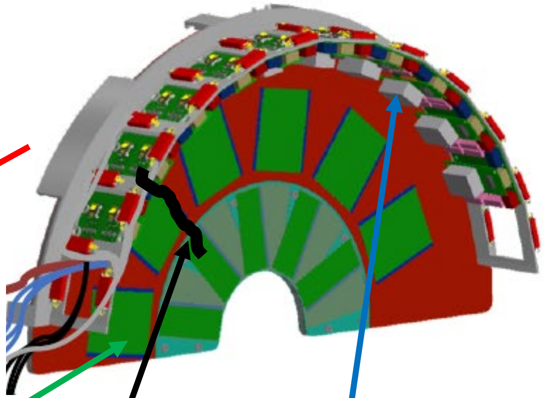





CALORIMETERS
ECAL Barrel
Replace FE electronics
New Endcap Calorimeters
Radiation tolerant - high granularity
Investigate coverage up to η ~ 4
MIP TIMING LAYERS
Barrel: LYSO + SiPM
Endcaps: Low Gain Avalanche Diode
NEW TRACKER
Radiation tolerant - high granularity - less material
Tracks in hardware trigger (L1)
Coverage up to η ~ 4
TRIGGER/DAQ
L1 (hardware) with tracks and rate ~750kHz
Latency ≥ 10 μs
HLT output up to 10 kHz
MUON
Replace DT FE electronics
Complete RPC coverage in forward region (new GEM/RPC technology)
Investigate Muon-tagging up to η ~ 4

On Detector Readout Chain



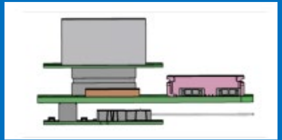


Forward disk
(TFPX)

Module with
readout chips
(ROCs)

e-link 1.28 Gbps

e-link 160Mbps



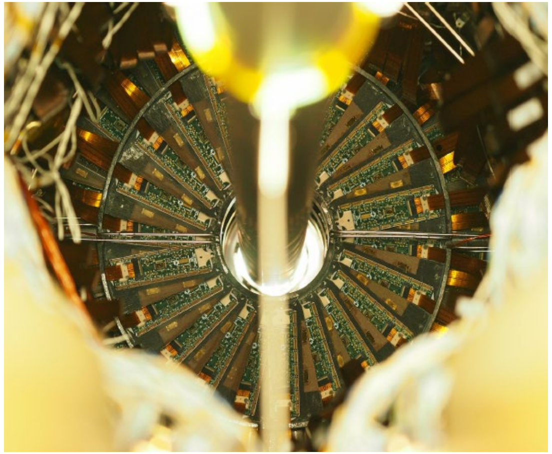
Portcard:
LpGBT, VTRx+ DC-DC

Optical fiber 10 Gbps

Optical fiber 2.5Gbps

Experimental Particle Physics and Detectors

Alice Bean
University of Kansas
Oct 20, 2022



We acknowledge funding support from the National Science Foundation